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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/629,640

07/29/2003

Maher Amer

13587.39

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12/04/2006

BERKELEY LAW & TECHNOLOGY GROUP
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EXAMINER

LAFORGIA, CHRISTIAN A

ART UNIT

PAPER NUMBER

2131

DATE MAILED: 12/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/629,640

Applicant(s)

AMER, MAHER

Examiner

Christian La Forgia

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 24 January 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-16 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-16 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 29 July 2003 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date <u>5/5/04</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. Claims 1-16 have been presented for examination.

Priority

2. Acknowledgment is made of applicant's claim for priority under 35 U.S.C. 119(e) to provisional application no. 60/411,343.

Information Disclosure Statement

3. The information disclosure statement (IDS) submitted on 05 May 2004 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the examiner has considered the information disclosure statement.

Drawings

4. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: on page 4, paragraph [0013] mentions system **10**, which does not appear in the drawings. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-7 and 13-16 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,355,415 to Lee et al., hereinafter Lee.

7. As per claim 1, Lee teaches a system for processing a set of data bits using a subset of a recurring sequence of scrambler bits, the system comprising:

receiving means for receiving said set of data bits (Figures 3B [input line for $\{b_k\}$], 4, column 4, lines 41-44, i.e. input data sequence);

storage means for storing said set of data bits (Figures 3B [input lines for $\{b_k^0, b_k^1, b_k^{n-1}\}$], 4, 6A [input lines for data sequence $\{b_k^0, b_k^1, b_k^{n-1}\}$], column 4, lines 55-57, i.e. parallel input data sequences);

digital logic means for determining an appropriate subset of said sequence of scramble bits (Figures 6A [blocks 61, 71], 8B, column 6, lines 17-20, i.e. state transition matrix);

generating means for generating said appropriate subset (Figures 6A [blocks 61, 72], 8B, column 6, lines 17-20, column 10, lines 6-51, i.e. generating parallel sequences for scrambling parallel input data sequences); and

digital operation means for performing a bitwise parallel digital operation between said appropriate subset and said set of data bits to produce an output set of data bits (Figures 3B, 6A [block 63], column 1, lines 4-12, column 6, lines 17-20, i.e. scrambling binary data and

generating parallel sequences for scrambling parallel input data sequences). Lee discloses on at least page 1053 of the IEEE publication entitled “Realizations of Parallel and Multibit-Parallel Shift Register Generators” that the parallel scrambling disclosed in the instant invention has been modified to be multibit-parallel scrambling.

8. Regarding claim 2, Lee teaches wherein said system scrambles said set of data bits using said appropriate subset of scramble bits (Figures 3B, 6A [block 63], column 1, lines 4-12, column 6, lines 17-20, i.e. scrambling binary data and generating parallel sequences for scrambling parallel input data sequences).

9. Regarding claim 3, Lee teaches wherein said system descrambles said set of data bits using said appropriate subset of scramble bits (Figure 6B [block 69], column 6, lines 30-57).

10. Regarding claims 4 and 10, Lee teaches wherein said receiving means comprises a multiplexer (column 4, lines 41-44, i.e. the input data sequence $\{b_k\}$ should be multiplexed to implement parallel distributed scrambling).

11. Regarding claim 5, Lee teaches wherein said digital logic means determines said appropriate subset based on an immediately preceding subset (Figures 6A [blocks 61, 71], 8B, column 6, lines 17-20, i.e. state transition matrix). Lee states at column 6, line 66 to column 7, line 2 that the state transition matrix can be obtained from D.W. Choi's publication “Parallel scrambling techniques for digital multiplexer,” hereinafter Choi. Choi states on page 124 that

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the state transition matrix is represented by matrix T (illustrated on page 124, 2nd column) and that given a current state and the state transition matrix one can predict the next state, therefore, teaching that said appropriate subset (next state) is based on the immediately preceding subset (i.e. current state).

12. With regards to claims 6 and 11, Lee teaches wherein said digital logic means is a combinational logic circuit (Figures 6A [blocks 61, 71], 8B, column 6, lines 17-20, i.e. shift register).

13. Regarding claims 7 and 9, Lee teaches wherein said bitwise parallel operation is a bitwise parallel XOR operation (Figures 3B, 6A [block 63], column 1, lines 4-12, column 6, lines 17-20). The symbol \oplus disclosed in Figures 2A, 2B, 3A, 3B, 6A, 6B, 8A and 8B is understood in logical terms to represent the exclusive-OR operation. The Lee reference states that for Figure 9, \oplus represents a modulo-2 adder.

14. As per claim 13, Lee teaches a method of processing a plurality of data bits using a subset of a recurring sequence of scrambler bits, the method comprising:

a) receiving (Figures 3B [input line for $\{b_k\}$], 4, column 4, lines 41-44, i.e. input data sequence) and storing in parallel said plurality of data bits (Figures 3B [input lines for $\{b_k^0, b_k^1, b_k^{n-1}\}$], 4, 6A [input lines for data sequence $\{b_k^0, b_k^1, b_k^{n-1}\}$], column 4, lines 55-57, i.e. parallel input data sequences);

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b) determining an appropriate subset of said sequence of scrambler bits based on an immediately preceding subset (Figures 6A [blocks 61, 71], 8B, column 6, lines 17-20, i.e. state transition matrix);

c) generating said appropriate subset (Figures 6A [blocks 61, 72], 8B, column 6, lines 17-20, column 10, lines 6-51, i.e. generating parallel sequences for scrambling parallel input data sequences);

d) loading said appropriate subset in a storage means (column 6, lines 24-28, i.e. the parallel sequences are obtained from the parallel shift register generator); and

e) performing a bitwise parallel XOR operation between said appropriate subset and said plurality of data bits (Figures 3B, 6A [block 63], column 1, lines 4-12, column 6, lines 17-20, i.e. scrambling binary data and generating parallel sequences for scrambling parallel input data sequences). Lee states at column 6, line 66 to column 7, line 2 that the state transition matrix can be obtained from Choi. Choi states on page 124 that the state transition matrix is represented by matrix T (illustrated on page 124, 2nd column) and that given a current state and the state transition matrix one can predict the next state, therefore, teaching that said appropriate subset (next state) is based on the immediately preceding subset (i.e. current state). The symbol \oplus disclosed in Figures 2A, 2B, 3A, 3B, 6A, 6B, 8A and 8B is understood in logical terms to represent the exclusive-OR operation. The Lee reference states that for Figure 9, \oplus represents a modulo-2 adder. The use of exclusive-OR operations is further supported by page 1058 of Lee's disclosure in the IEEE publication entitled "Realizations of Parallel and Multibit-Parallel Shift Register Generators."

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15. Regarding claim 14, Lee teaches wherein step b) is accomplished by performing logical operations between specific scrambler bits of said immediately preceding subset (Figures 6A [blocks 61, 71], 8B, column 6, lines 17-20, i.e. state transition matrix). Lee states at column 6, line 66 to column 7, line 2 that the state transition matrix can be obtained from Choi. Choi states on page 124 that the state transition matrix is represented by matrix T (illustrated on page 124, 2nd column) and that given a current state and the state transition matrix one can predict the next state, therefore, teaching that said appropriate subset (next state) is based on the immediately preceding subset (i.e. current state).

16. Regarding claim 15, Lee teaches wherein step c) is accomplished by performing logical operations between specific scrambler bits of said immediately preceding subset (column 6, line 66 to column 7, line 2, i.e. the parallel sequence generating vector). Lee states at column 6, line 66 to column 7, line 2 that the parallel sequence generating vector can be obtained from Choi. Choi states on pages 124 and 125 that parallel sequence generating vector basis the next parallel sequence on the current parallel sequence.

17. Regarding claim 16, Lee teaches wherein said storage means is a register (column 6, lines 24-28, i.e. the parallel sequences are obtained from the parallel shift register generator).

Claim Rejections - 35 USC § 103

18. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

19. Claims 8-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee in view of U.S. Patent No. 5,530,959 to Amrany, hereafter Amrany.

20. As per claim 8, Lee teaches a digital scrambler/descrambler using a subset of a securing sequence of scrambler bits, the scrambler/descrambler comprising:

digital logic means for determining an appropriate subset of said sequence of scrambler bits, said appropriate subset being determined based on an immediately preceding subset of said sequence of scrambler bits (Figures 6A [blocks 61, 71], 8B, column 6, lines 17-20, i.e. state transition matrix);

digital operation means for executing a bitwise parallel digital operation between said appropriate subset and said data set (Figures 3B, 6A [block 63], column 1, lines 4-12, column 6, lines 17-20, i.e. scrambling binary data and generating parallel sequences for scrambling parallel input data sequences). Lee states at column 6, line 66 to column 7, line 2 that the state transition matrix can be obtained from Choi. Choi states on page 124 that the state transition matrix is represented by matrix T (illustrated on page 124, 2nd column) and that given a current state and the state transition matrix one can predict the next state, therefore, teaching that said appropriate subset (next state) is based on the immediately preceding subset (i.e. current state).

21. Lee does not teach selection means for selecting between a first set of data bits to be scrambled and a second set of data bits to be descrambled.

22. Amrany discloses a selection means (Figures 4 [blocks 408, 428], 5 [block 428], 6 [block 428], column 3, lines 40-59, column 4, lines 24-53).

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23. Lee and Amrany are related in their field of endeavors as they are both related to self-synchronizing scrambling of data. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the selection means of Amrany in the system of Lee, since Amrany states at column 3, lines 37-39 that using a selector avoids using synchronization signals which are difficult and expensive to implement, especially in high speed communications.

24. With regards to claim 12, Lee teaches wherein said digital logic means includes a digital storage means for storing said immediately preceding subset (Figures 6A [blocks 61, 71], 8B, column 6, lines 17-20, i.e. shift register).

Conclusion

25. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

26. The following patents are cited to further show the state of the art with respect to parallel scrambling, such as:

United States Patent No. 5,241,602 to Lee et al., which is cited to show a parallel scrambling system.

United States Patent No. 5,488,661 to Matsui, which is cited to show a scrambling system with selection means.

United States Patent No. 7,106,859 to Myszne, which is cited to show a parallel data scrambler with selection means.

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United States Patent No. 7,133,432 to Kuffner et al., which is cited to show a recursive data scrambling system.

United States Patent No. 7,099,469 to Kuhlman et al., which is cited to show a recursive data scrambling system.

United States Patent Application Publication No. 2003/0145196 to Heegard et al., which is cited to show a self-synchronizing data scrambling system.

United States Patent No. 4,744,104 to Pospischil, which is cited to show a self-synchronizing scrambler.

United States Patent No. 4,807,290 to Pospischil, which is cited to show a self-synchronizing scrambler.

United States Patent No. 5,844,989 to Nishida et al., which is cited to show a parallel bitwise scrambler.

United States Patent No. 5,966,447 to Nishida et al., which is cited to show a parallel bitwise scrambler.

United States Patent No. 5,978,486 to Nishida et al., which is cited to show a parallel bitwise scrambler.

United States Patent No. 5,377,265 to Wettengel et al., which is cited to show a parallel additive scrambler.

United States Patent No. 6,888,943 to Lam et al., which is cited to show a multimedia scrambling.

United States Patent No. 5,844,989 to Nishida et al., which is cited to show a parallel bitwise scrambler.

United States Patent No. 3,784,743 to Schroeder, which is cited to show a parallel data scrambler.

United States Patent No. 5,267,316 to Merino Gonzalez et al., which is cited to show a synchronous parallel scrambler.

United States Patent No. 6,414,957 to Kang et al., which is cited to show a distributed sample scrambler.

United States Patent No. 5,231,667 to Kojima, which is cited to show a parallel scrambler manufactured as a CMOS arrangement in LSI format.

United States Patent Application Publication No. 2004/0025104 to Amer, which is cited to show a similar, commonly owned system used for error correction.

27. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christian La Forgia whose telephone number is (571) 272-3792. The examiner can normally be reached on Monday thru Thursday 7-5.

28. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ayaz Sheikh can be reached on (571) 272-3795. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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29. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Christian LaForgia
Patent Examiner
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A handwritten signature in black ink, appearing to read 'Christian LaForgia', written over a horizontal line.

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